Bhushan (Vidyabhushan) Mohan

CONTACT mohan@cs.virginia.edu, mailtovb@gmail.com

INTERESTS Hardware system design, performance analysis and computer architecture.

EDUCATION **University of Virginia**, Charlottesville, Virginia USA

Doctor of Philosophy, Computer Science, 2010 - 2015

- Dissertation: *Towards Building Energy Efficient, Reliable, and Scalable NAND Flash Based Storage Systems*
- Advisors: Kevin Skadron and Mircea R. Stan

M.S., Computer Science, 2008 - 2010

- Thesis: *Modeling the Physical Characteristics of NAND Flash Memories*
- Advisor: Sudhanva Gurumurthi

College of Engineering, Guindy, Anna University, Chennai, India

B.E., Computer Science and Engineering, 2002 - 2006

- Thesis: *Implementation of .NET CLR on FPGAs*
- Advisor: Professor Ranjani Parthasarathi

PROGRAMMING LANGUAGES Python, C.

EXPERIENCE **Member of Technical Staff**, Pure Storage, October 2018 - Present

As a software engineer in the Hardware Analytics team, I build data pipelines to monitor the performance and reliability of millions of Pure's products deployed in the field. I build tools that use telemetry from these products to provide early warning of various failures. Engineering and sales team proactively address these failures, thereby ensuring that customer data is always protected and our products meet high quality standards.

Research Engineer (various levels), Enterprise Storage Advanced Technology - Western Digital, March 2013 - October 2018

As a storage system architect in the advanced architecture team, I built pre-silicon behavioral models of enterprise SSDs, instrument and analyze performance of post-silicon product samples, and generally explore the design space of storage systems. I built data pipelines and analysis frameworks that mine metadata extracted from product samples and quickly identify and solve performance bottlenecks.

Intern, Rambus Labs, May 2012 - March 2013

Developed circuit and architecture level models to study the performance, area, and power consumption of various Resistive RAM (ReRAM) memory technologies. Used these models to evaluate placement of these technologies at various levels in the memory hierarchy. Proposed and evaluated a gigascale last level cache that decoupled tag and data array design to improve performance efficiency.

Research Assistant, Computer Science, University of Virginia. January 2009 - May 2012

My dissertation addresses the power, reliability and scalability challenges of NAND flash based storage systems by modeling the metrics, evaluating the tradeoff between the metrics and exploring the design space to build application optimal storage systems. I also worked on redesigning the memory hierarchy with Storage Class Memory (SCM) technologies like Spin Torque Transfer RAM (STT-RAM). I have been part of the following projects:

- NAND Power Modeling - [TCAD 2013, DATE 2010]: Developed *FlashPower*, a detailed analytical model for flash memory chip energy dissipation. Validated the model with data from real chip measurements and used the model to optimize memory architecture for power consumption.
- NAND Reliability Modeling - [HotStorage 2010, Techreport 2012, Flash Memory Summit 2012]: Developed *FENCE*, an analytical model to understand the factors affecting NAND reliability. Used the model to quantify the impact of system operating conditions like write frequency and temperature on flash failure mechanisms like endurance and data retention.
- Improving Endurance of Data center SSDs - [Techreport 2012, Flash Memory Summit 2012]: Proposed and evaluated novel SSD firmware algorithms that exploit trade-offs between endurance and data retention to increase endurance of data center SSDs.
- Cache design using STT-RAM - [HPCA 2011, ISLPED 2011]:Explored architecture and circuit level techniques that reduce the write energy and latency of STT-RAM and use them to design caches.

Intern, Platforms - Data center Storage, Google Inc, May 2011 - Aug 2011

I built analytical models to capture the effect of Program/Erase (P/E) cycles on the Raw Bit Error Rate (RBER) of $34nm$ and $22nm$ flash technology. I used these models in conjunction with the reliability data extracted from SSDs deployed in Google's data center to characterize and predict SSD lifetime.

Member Technical Staff, Adobe Systems, India. July 2006 - July 2008

Product Developer for the Mobile and Devices Business Unit, involved in the development of Flash Lite™, a version of Adobe® Flash™ Player optimized to run on mobile devices. I have been part of the following projects:

- Flash Lite Player Security - Designed and developed security features for Flash Lite versions 3.1 and 3.1.5.
- Web-browsability - Enabled Flash Lite powered mobile devices to render flash player content in web pages.
- Flash Lite Plug-in for Internet Explorer Mobile - Ported the Flash Lite interface to Internet Explorer Mobile to facilitate web browsing in Windows Mobile Phones.

PUBLICATIONS

Vidyabhushan Mohan, Trevor Bunker, Laura Grupp, Sudhanva Gurumurthi, Mircea R. Stan and Steven Swanson. Modeling Power Consumption of NAND Flash Memories Using FlashPower. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Issue 7, July 2013.

Anurag Nigam, Clint Smullen, **Vidyabhushan Mohan**, Eugene Chen, Sudhanva Gurumurthi and Mircea R. Stan. Delivering on the Promise of Universal Memory for Spin-Transfer Torque RAM (STT-RAM). In: *International Symposium on Low Power*

Electronics and Design (ISLPED). Fukuoka, Japan. August 2011. **Acceptance Rate: 23%**.

Clint Smullen, **Vidyabhushan Mohan**, Anurag Nigam, Sudhanva Gurumurthi and Mircea R. Stan. Relaxing Non-Volatility for Fast and Energy Efficient STT-RAM Caches. In: 17^{th} *IEEE Symposium on High Performance Computer Architecture (HPCA 17)*. San Antonio, TX. February 2011. **Acceptance Rate: 19%**.

Vidyabhushan Mohan, Taniya Siddiqua, Sudhanva Gurumurthi and Mircea R. Stan. How I Learned to Stop Worrying and Love Flash Endurance. In: 2^{nd} *Workshop on Hot Topics in Storage and File Systems (HotStorage)*. Boston, MA. June 2010. **Acceptance Rate: 31%**.

Vidyabhushan Mohan, Sudhanva Gurumurthi and Mircea R. Stan. FlashPower: A Detailed Power Model for NAND Flash Memory. In: *Design Automation and Test in Europe (DATE)*. Dresden, Germany. March 2010. **Acceptance Rate: 30%**.

TECHNICAL REPORTS

Vidyabhushan Mohan, Sriram Sankar and Sudhanva Gurumurthi. reFresh SSDs: Enabling High Endurance, Low Cost Flash in Datacenters. University of Virginia, Technical Report, CS-2012-05. May 2012.

POSTERS

Vidyabhushan Mohan and Sudhanva Gurumurthi. Tools for Architecture-level Design and Analysis of Flash Memory Systems. In: 2^{nd} *Annual Non-Volatile Memories Workshop (NVMW)*. San Deigo, CA. March 2011.

Srinath Sridharan, Srinivasan Thirunarayanan and **Vidyabhushan Mohan**. Implementation of .NET CLR on FPGAs. In: 12^{th} *International Conference on High Performance Computing (HiPC)*. Goa, India. December 2005.

AWARDS

L.William Ballard Jr. Fellowship, School of Engineering and Applied Sciences, University of Virginia, 2011.

Dean's Fellowship, University of Virginia, 2008.